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Implementation of Fundamental Modules Using Quantum Dot Cellular Automata

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Abstract

This paper aims to design logic gates and flip flops using QCA. This paper demonstrates the implementation of logic gates. (AND GATE, OR GATE, NOR GATE, NOT GATE, EXOR-GATE, X-NOR GATE, NAND GATE) and flip flops (SR flip flop, JK flip flop, D flip flop and T flip flop) using QCA designer tool software. Using QCA, we can reduce power dissipation, increase the speed of operation, and decrease area size. QCA is known as Quantum Dot Cellular Automata, and it is a transistor less model. We don't need transistors, resistors& capacitors to build or design any logic gates and flip flops. QCA is a square shape nano-structure that can perform computations. Instead of transferring information through current and voltage, it transfers the information in the form of polarization. The QCA cell basic structure consists of four quantum dots and two electrons. These two electrons can occupy any of the four quantum dots and tunnel between them but can't come out due to high barrier potential.

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Introduction

This paper aims to design logic gates and flip flops using QCA. This paper demonstrates the implementation of logic gates (AND GATE, OR GATE, NOR GATE, NOT GATE, X-OR GATE, X-NOR GATE, NAND GATE) and flip flops (SR flip flop, JK flip flop, D flip flop and T flip flop) using QCA designer tool software. Moore's law has started to fail. It is not, at this point, substantial to foresee the speed and size of electronic gadgets due to lithography issues, high leakage current, doping fluctuations, as the channel of transistors are short scaling not possible.

Using QCA, we can reduce power dissipation, increase the speed of operation, and decrease area size. QCA is known as Quantum Dot Cellular Automata, and it is a transistor less model. To implement any logic circuits like gates and flip-flops, we don't need any transistor, resistor, capacitor. QCA is a square shape nano-structure that can perform computations. Instead of transferring information through current and voltage, we transfer data in the form of polarization. The QCA cell contains four quantum dots at the ends of the cell and two electrons. These two electrons occupy any of the four quantum dots and tunnel between them, but they can't come out due to high barrier potential.

QCA is a recent advancement in Nano-electronics that has progressed technologically to simulate multidimensional quantum circuits and equipment. In contrast to traditional computers, QCA represents digital information as a combination of electron pairs associated with quantum dot arrays. Quantum dots are used in QCA designer to implement Boolean logic. Digital circuits built with QCA have a massive length reduction and, as a result, location discount and a high speed at reduced power levels.[1]. State changes in QCA occur due to interactions between neighboring cells caused by an electrostatic or electromagnetic field.

Consequently, in QCA, electron positions reflect values in quantum dots rather than using voltage and current ranges to indicate binary values in conventional computers. QCA circuits are being built at densities up to 1014 cells/cm2, and the switching frequency of the circuit is rapidly approaching a terahertz. Even though it has advantages like stability, excessive velocity, reduced space, and lower power intake. QCA circuits lack design types of equipment. Machines that help in the layout and computation of significant electronic components and circuit manufacturing contribute to the advancement of nano-electronic technology.

A. Conventional Method

CMOS stands for "Complementary Metal Oxide Semiconductor". Designers used CMOS technology to build integrated circuits; CMOS technology is the most popular technology. Due to the advantages of CMOS, many electronic devices make use of this technology. Capacitors, diodes, and other components are needed to develop integrated chips, which increases chip size, power dissipation & complexity of the circuit also increases. Due to high power dissipation, the circuit gets damaged, and it needs to be replaced. For different logic function, this technology employs both PMOS & NMOS.

Frank Wanlass, who worked at the Fairchild semiconductor, invented CMOS technology in 1963. NMOS& PMOS are used in CMOS. In general, CMOS technology is connected with VLSI, which integrates millions and billions of transistors on a single chip. CMOS technology is popular in the fabrication of VLSI chips is reliability, low power consumption and scalability.

Logic gates were implemented using NMOS and PMOS before CMOS. PMOS was gradually replaced by NMOS, which was once an industry standard for the fabrication of Integrated circuits. CMOS was slower and more expensive than NMOS in the initial days. Simple operation, processing speed and manufacturing efficiency are advantages of NMOS. The main drawbacks of NMOS circuits are static power dissipation and high electrical asymmetry. High usage, lower speed, and density beyond 10 nm have restricted CMOS technology in recent years. To solve these problems, a group of researchers are focusing on developing alternative for this traditional CMOS technology known as Quantum-dot cellular automata, which are used for high-speed applications.

Proposed Design

In 1993, Craig Lent developed a technology called quantum-dot cellular automata. This new technology has replaced silicon-based CMOS technology. In general, QCA employs an array of combined quantum dots to implement various Boolean logic. In QCA, a cell is a fundamental element. The logical bit representation in the QCA cell is accomplished by adjusting the charge configuration. Each quantum cell is made up of four quantum dots that are placed at the edges of a square structure. When it comes to scaling, Quantum dot is a Nano-structure that investigates properties of quantum mechanics. The four quantum dots represent a QCA cell. In these four dots, electrons pairs occupy any position oppositely diagonally. Electron pairs occupy opposite position diagonally rather than neighbouring places due to less Columbic repulsion. Tunnel junctions bind these dots in a cell. In a cell, information is passed in polarization instead of transferring the data through current or voltage. The polarization is divided into two types based on electrons' position, i.e. polarization P=-1 and polarization P=+1. P=-1 is represented as logic 0, and P=+1 is represented as logic 1 (Figure 1).

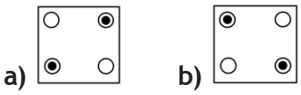

Fig. 1: QCA cell with polarization. (a). P=-1(Logic 0). (b). P=-1(Logic 0).

$$p = \frac{(p_1 + p_3) - (p_2 + p_4)}{(p_1 + p_2 + p_3 + p_4)} \quad (1)$$

The polarization of two cells is influenced when they are placed near each other. When many quantum cells are put together, they form a wire. This polarization of the second cell is affected by the polarization of the first cell. The second cell near the first cell will have the same polarization as the first cell to reduce Coulomb interactions (Figure 2).

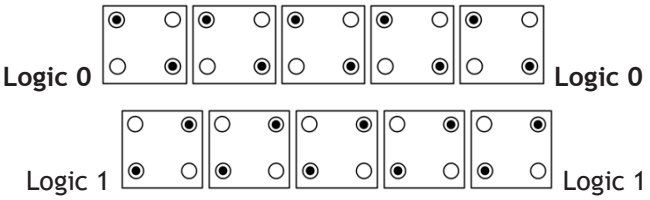

Fig. 2: Quantum cell wire.

A. Clocking in QCA

The QCA clock not solely synchronizes and controls data; however, it also provides power to the circuit. For clocking a QCA cell, a four-phase clocking method is employed; changing the clock phase; signal strength can be restored. The four phases are switch, hold, release, relax with a 90 degree lag between them. To ensure that data is propagated through QCA with no unexpected changes of QCA cells, a clock should be designed to ensure similar information is placed from input to output (Figure 3 & Table 1).

The QCA cell does not begin polarized and advances to a spellbound state while the potential boundary is enhanced from low to high during the clock's "Switch" stage (Figure 4). The polarization state is equivalent to the past advance, and the potential border is solid during the "Hold" stage. The potential obstruction is brought down in the "Release" measure, and the cells become

Unpolarized. During the "relax" stage, the potential boundary stays brought down, and the phones remain non-polarized. The cells are currently ready to switch once more. In QCA circuits, data is engendered in this route by keeping up the ground-state polarization consistently.

Implementation Of Logic Gates & Flip-Flops Using QCA

A. Inverter (Not Gate)

Inverter or not Gate is a logic device that produces complementary or inverting output to the given input, i.e. when logic one is given as the input. The output obtained by the not Gate is logic 0; similarly, when logic 0 is given as input, then output obtained is logic "1". NOT Gate is implemented by aligning two cells at a 45-degree angle to function in the opposite direction (Table 2 and Figure 5).

B. AND Gate

If both inputs are high, the AND Gate provides high output. In other words, if one of two inputs is low, the output is logic 0. In QCA, the AND Gate is implemented by adjusting any of the majority gate's inputs to 0 (polarization=-1) (Figure 6).

The expression of AND Gate is M(a,b,0)=ab

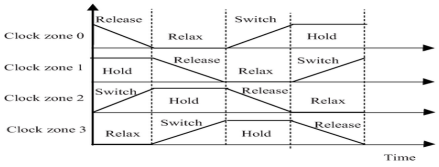

Fig. 3: Phases of QCA clock

Table 1: QCA Clock Phases Operation

Clock Phase	Potential barrier	Polarization of the cells
Hold	Held high	Polarized
Switch	Low to high	Polarized
Relax	Low	Unpolarized
Release	Lowered	Unpolarized

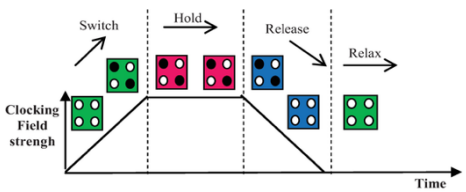

Fig. 4: Inter-dot barriers of QCA clock.

C. OR Gate

OR Gate is a logic device that produces logic high output if either of the inputs is high. It has logic 0 if both the input signals are low, i.e. a=b=0. OR Gate is implemented in QCA by making any of the inputs of the majority gate as one, i.e. (polarization=+1) (Figure 7).

The expression of OR gate is M(a,b,1)=a+b

D. NAND Gate

NAND gate is a logic device that produces logic high, i.e. (logic 1) if any one of the inputs is low and when both the inputs are high, it has a logic low signal, i.e. (logic '0'). NAND gate is implemented in QCA by inserting a not gate or inverter at the output stage of AND Gate. Expression of NAND gate is Y=(AB)' (Figure 8).

E. NOR Gate

NOR Gate is a logic device that produces logic high, i.e. logic one if applied inputs are low (A=B=0) and produces logic low signals in the remaining conditions. NOR Gate is implemented in QCA by placing not Gate or Inverter at the output stage of the OR gate. The expression of NOR gate is Y=(a+b)' (Figure 9).

Table 2: Characteristic table of Inverter

A	Y=A'
0	1
1	0

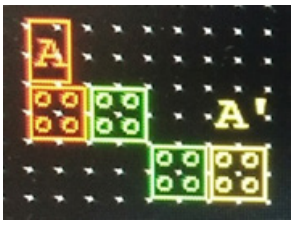

Fig. 5: NOT Gate implementation in QCA

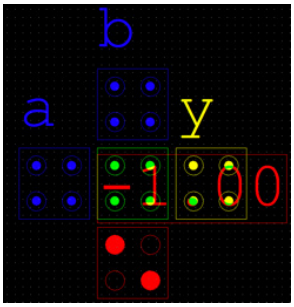

Fig. 6: AND Gate implementation in QCA

F. EX-OR Gate

Exclusive – OR Gate is also known as EX-OR Gate. If both inputs are different, It has a logic. It is a logic circuit that produces logic high output, i.e. (logic 1) when both the inputs are different. It has a logic low output while both inputs are the same, i.e. (logic 0) (Figure 10).

G. EX-NOR Gate

EX-NOR Gate is also known as Exclusive – NOR Gate. It is a logic circuit that produces logic high, i.e. (logic 1). Suppose the given inputs are the same. It produces logic low output when the inputs are different (logic 0).implementation of EX-NOR gate in QCA by placing an inverter at the end of the ex-or output. The expression of EX-NOR gate is Y=(a b)' (Figure 11).

Flip-Flop Implementation

A. SR Flip-flop:

Set-reset flip-flop is abbreviated as SR flip-flop. It consists of two inputs, i.e. set & reset and two outputs Q and QB (Figure 12).

Operation: 1. When the clock pulse is low =0, the output doesn't change, i.e. the response is similar to the previous output. 2. When the clock pulse is high=1 then

a. When both the inputs S=0, R=0, the output doesn't change, i.e. output, is similar to the previous output.
b. If inputs S=1 & R=0, then the output is set(Q=1 and QB=0).
c. If inputs S=0 & R=0, then the output is reset (Q=0 and QB=1).
d. When both the input S= 1 and R=1, then the output is invalid.

B. JK- Flip-Flop

The Revised form of SR Flip-Flop is JK Flip-Flop. When compared to SR Flipflop intermediate condition of the JK flip-flop is more accurate. Based on input characteristics, JK and SR flip-flops are the same. The letter J indicates SET, and letter K indicates RESET (Figure 13).

Expression of JK Flip-Flop is Qn+1 = J.Qn'+K'Qn

a. J=K=0: When both inputs are zero, then output doesn't; it is similar to the previous output, i.e. If the preceding output is high, then the current state output is also high, vice-versa.
b. J=0, K=1: If J=0 and K=1 then the output is reset (Q=0 & Q'=1). If the applied clock signal is in a high state, the output will be 0 & if it is in a low state, the output will be the same as the previous state.

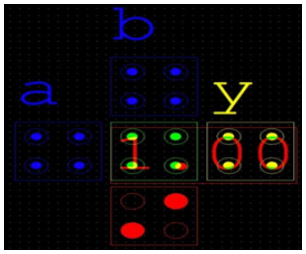

Fig. 7: OR Gate implementation using QCA

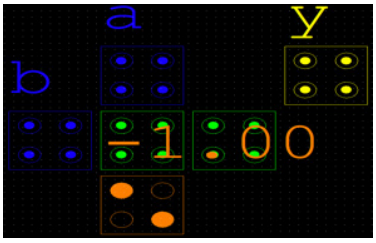

Fig. 8: NAND Implementation using QCA

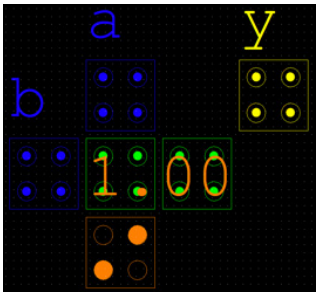

Fig. 9: NAND Implementation using QCA

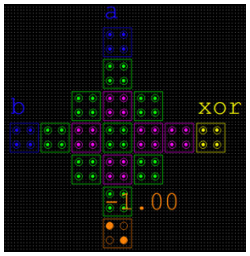

Fig. 10: Ex-or Gate implementation in QCA

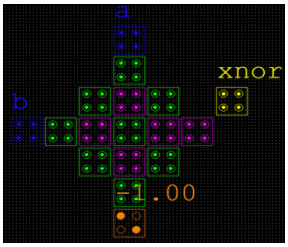

Fig. 11: Ex-nor Gate implementation in QCA.

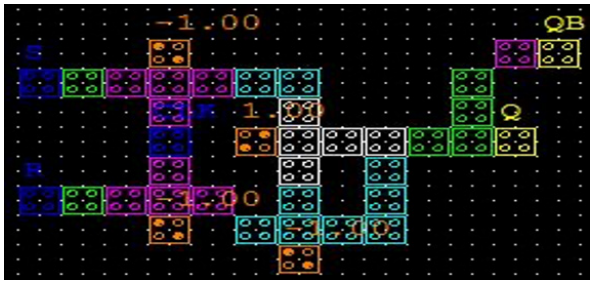

Fig. 12: SR Flip-Flop QCA implementation.

c. J=1, K=0: If J=1&K=0 then the output is SET i.e 1
d. J=K=1: When both inputs J=K=1 on the present state output, there is a possibility of a set or reset, i.e. the output toggles.

C. T flip-flop

Toggle flip-flop is another name of T Flip-flop. It can be built from the JK flip-flop by connecting the J&K pins. Hence it is also known as the single input version of the JK flip-flop. If the clock pulse is applied to the flip-flop, at half the frequency of the input T, the output begins to toggle. The response of T flip-flop is the EX-OR operation between T and Qn (Figure 14).

The expression for T flip-flop is T'Q+TQ'= T XOR Q

a. If the clock is low and T=0, there won't be any change in the output of the present state, i.e. no Change.
b. If the clock is high and T=1, the output toggles between 0 and 1.

D. D Flip-Flop:

Delay Flip-Flop is another name of D-flipflop. It introduces a delay between outputs and inputs. The D Flip-flop is constructed by attaching S and R terminals of the SR flip-flop with an inverter. The information at D is delayed by one clock pulse at the output (Figure 15).

a. If input D is 0, then the flip-flop output is reset.
b. If input D is 1, then the flip-flop output is set

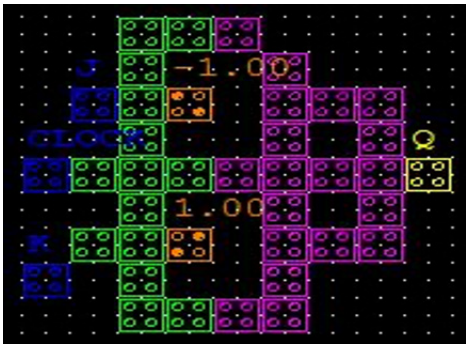

Fig. 13: JK Flip-flop implementation using QCA

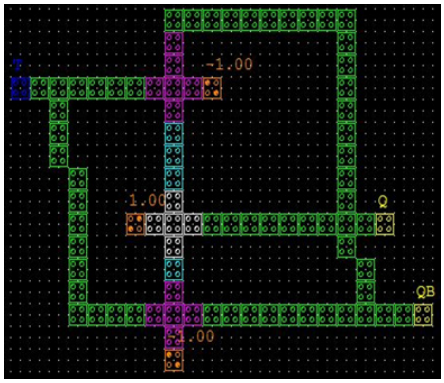

Fig. 14: T Flip-flop implementation using QCA.

Simulation Results & Experimental Findings Of The Proposed Work

The results obtained after the simulation of all essential Gates and flip-flops are presented below.

Fig. 16(a) simulation result of the inverter explains the operation of the inverter, which is given in table 2. i.e. if the given input is zero, the output generated by the inverter is logic one. Here the input is represented in blue colour, and output is represented in yellow colour. When the input is low, the output obtained is high.

Fig. 16(b) is the simulation result of the AND Gate; it obeys the characteristic table of AND Gate table3, i.e. when both the inputs are high, the output obtained by the Gate is high. If any of the input is low, the result obtained is low I,e zero. This output is observed in the above figure, i.e. when two inputs are high, the output is also high in remaining conditions, the result is low. Fig. 16(c) is the simulation result of the OR gate, and it obeys the characteristic table of OR gate table4, i.e. if any of the one input is high, the output of the or Gate is high; in the remaining cases, the result obtained is low. This output is observed in the above figure, i.e. when any of the input is high, the OR gate's output is high and low in the remaining cases.

Fig. 16(d)is the simulation result of the NAND Gate; it obeys the characteristic table of NAND Gate table5, i.e. when both the inputs are high, the output obtained

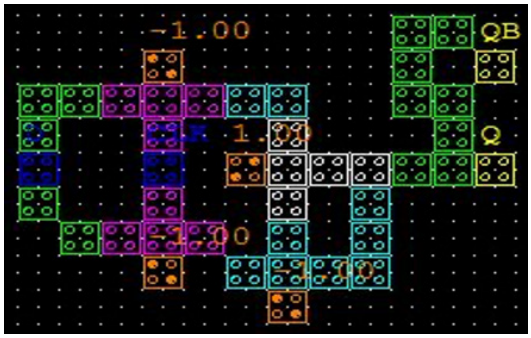

Fig. 15: D flip-flop implementation using QCA.

Table 3: Parameters observed in designing gates in QCA

Size of cell	18 nm
amplitude of clock	2.0000
high	9.8000e−022 J
low	3.8000e−023J
Maximum iterations per sample	100
Radius of effect	65.0000 nm
Convergence tolerance	0.0000100
Number of samples	50000
Relative permittivity	12.9.

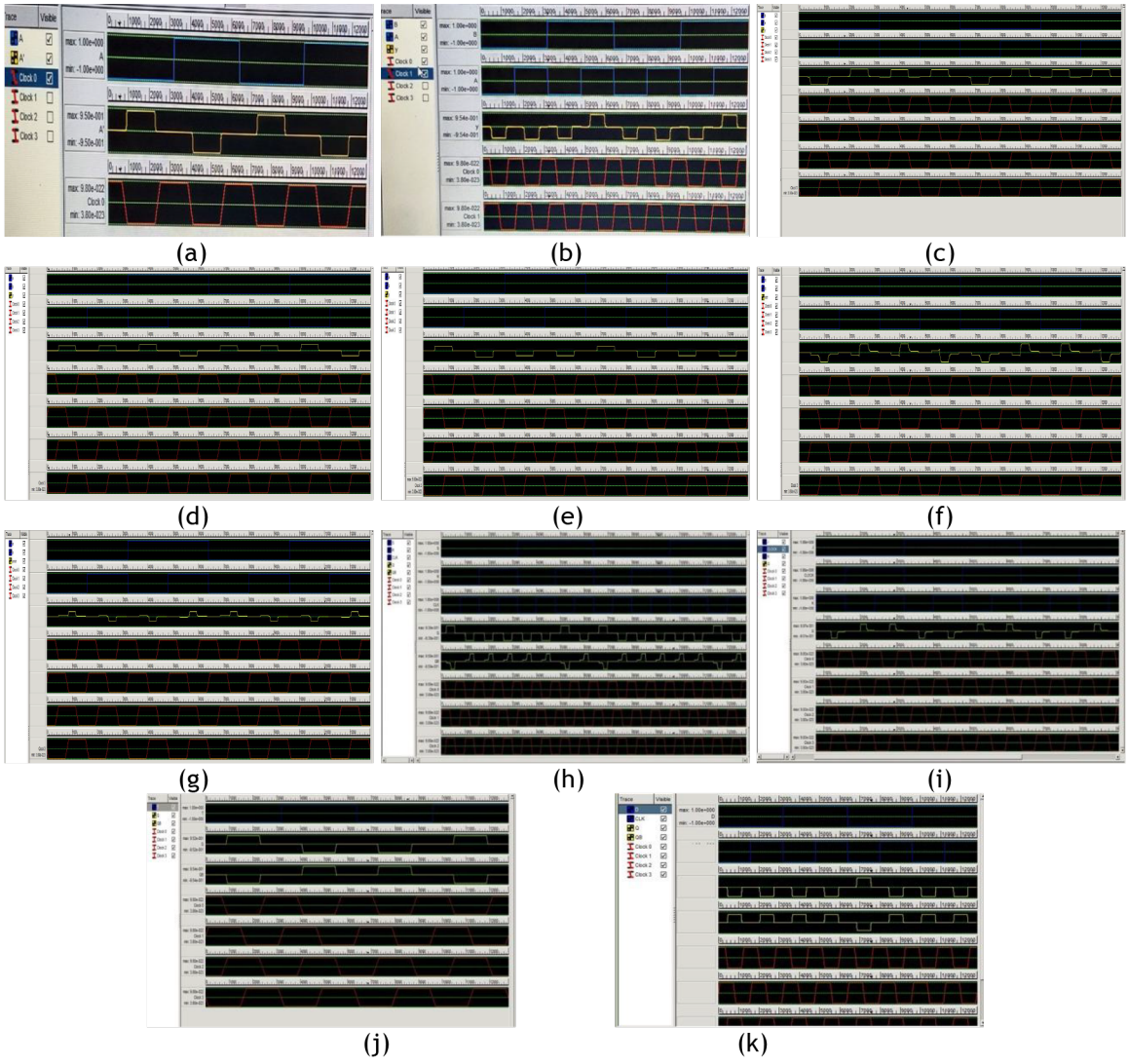

Fig. 16: Simulation Results of QCA based logic gates showin Figs. 5-15.

by the Gate is low. If any of the input is low, the result obtained is high I,e logic one this output is observed it in the above figure, i.e. when two inputs are high, the output is low in remaining conditions the result is high. Fig. 16(e) is the simulation result of the NOR gate, and it obeys the characteristic table of NOR gate table6, i.e. if both inputs are low, the output of the NOR Gate is high; in the remaining cases, the result obtained is low. This operation is observed in the above figure, i.e. When both inputs are common, the output of the NOR gate is high, and in the remaining cases, the output is low.

Fig. 16(f)is the simulation result of the EX-OR gate. It obeys the characteristic table of EX-OR gate table7, i.e. if both the inputs are different, the output of the EX-OR gate is high; in the remaining cases, the output is low. This operation is observed in the above Fig.. Fig. 16(g) is the simulation result of the EX-NOR gate. It obeys the characteristic table EX-NOR gate table 8, i.e. if both inputs are the same, the output of the ex-nor Gate is high. In other cases, the result is low. This operation is observed in the above Fig. 16.

Fig. 16(h) is the simulation result of the SR Flip-Flop. It obeys table 9. When the clock pulse is low, the output doesn't change, i.e. the response is similar to the previous output. When the clock pulse is high, and the inputs S=0, R=0, the output doesn't change, i.e. output, similar to the previous output.If inputs S=1 & R=0, then the output is set(Q=1 and QB=0).If inputs S=0 &R=0, then the output is reset (Q=0 and QB=1).When both the input S= 1 and R=1, then the output is invalid. This operation is observed in the above Fig. 16.

Fig. 16(i) is the simulation result of the JK Flip-flop. It obeys table 10. If j=k=0, i.e. both inputs are zero, then output doesn't change; it is similar to the previous output, i.e. If the preceding output is high, then the current state output is also high, vice-versa. If J=0 and K=1, then the output is reset (Q=0 & Q'=1). If the applied clock signal is in a high state, the output will be 0 & if it is in a low

condition, the output will be the same as the previous state. If J=1&K=0, then the output is SET, i.e. 1. If both inputs J=K=1 on the present state output, there is a possibility of a set or reset, i.e. the output toggles.

Fig. 16(j) is the simulation result. It obeys table 11. If the clock is low and T=0, there won't be any change in the output of the present state, i.e. no Change. If the clock is high and T=1, the output toggles between 0 and 1. Fig. 16(k) is the simulation result of the D flip-flop. It obeys table 12. If input D is 0, then the flip-flop output is reset. If input D is 1, then the flip-flop output is set.

Conclusion

This paper has presented several implementations of logic gates and flip-flop using Quantum-dot cellular automata technology. The reduction of the number of required cells is an essential step in the design of QCA circuits. Compared to CMOS technology, these designs provide better results in small areas, high speed, high frequency and low power computation.

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